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MK Svancarek, ME Adan, MW Van Flandern, JG Pierce, ... - US Patent 5,793,356, 1998 -

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... SOFTWARE EMULATION OF A COMPUTER ... host computer may have bidirectional communication

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Y.Kaneda, H.Takahashi, M.Saito, H.Aida, H.Tokuda - Proceedings of 4th ACM SIGCOMM workshop on Network and ..., 2005 - portal.acm.org

... it is difficult to continue hosting a gaming ... The port number and the binary name are described ... contexts by appending each message to context information. ...

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MK Svancarek, ME Adan, MW Van Flandern, H.Suzuki - US Patent 5,628,686, 1997 - Google Patents

... that a significant amount of computer processing time is ... Thus, the host computer must spend a significant amount of time ... designated as binary devices since they typically ...

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S.Zdenek - Discourse & Society, 1999 - das.sagepub.com

... p. 12) implies an ongoing, highly regulated, process of identity ... coy', but 'usually divulges information if one ... ent across Mauldin's binary gender system ...

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MK Svancarek, ME Adan, MW Van Flandern, H Suzuki - US Patent 5,724,558, 1998 - Google Patents

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B Strategies - tuta.hut.fi

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INFORMATION AND

CONTENT (Non-Voice ... also possible to download an **emulator**-software called GoBoy ...

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G Accessibility, F ActiveX, M Mail - language - media.wiley.com

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hosts.deny file ... VPN, configuration, 673-676 contact **information**, domain name ...

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1 [Analysis of hardware and software approaches to embedded in-circuit emulation of microprocessors](#)

Hsin-Ming Chen, Chung-Fu Kao, Ing-Jer Huang

 January 2002 **Australian Computer Science Communications , Proceedings of the seventh Asia-Pacific conference on Computer systems architecture CRPIT '02**, Volume 24 Issue 3

Publisher: Australian Computer Society, Inc., IEEE Computer Society Press

 Full text available: [pdf\(665.32 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper investigates various approaches to embed the functionality of in-circuit emulation (ICE) into microprocessor cores in SoC (System-On-Chip) chips. Three styles of ICE's (hardware-oriented, software-oriented and hybrid) are defined and implemented. They are integrated with a synthesizable ARM7 microprocessor core and synthesized to gate level to quantitatively analyze and compare their performance, cost and debugging features.

2 [Session 36: electrical and thermal issues in FPGAs: A fast HW/SW FPGA-based](#)

[thermal emulation framework for multi-processor system-on-chip](#)

David Atienza, Pablo G. Del Valle, Giacomo Paci, Francesco Poletti, Luca Benini, Giovanni De Micheli, Jose M. Mendias

 July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

 Full text available: [pdf\(1.34 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

With the growing complexity in consumer embedded products and the improvements in process technology, Multi-Processor System-On-Chip (MPSoC) architectures have become widespread. These new systems are complex to design as they must execute multiple complex applications (e.g. video processing, 3D games), while meeting additional design constraints (e.g. energy consumption or time-to-market). Moreover, the rise of temperature in the die for MPSoC components can seriously affect their final perform ...

Keywords: FPGA, MPSoC, emulation, thermal studies

3 [Emulation of computer networks by microprogrammable microcomputers](#)

David Cohen, Ming T. Liu

 September 1974 **Conference record of the 7th annual workshop on Microprogramming MICRO 7**

Publisher: ACM Press

Full text available:  pdf(430.27 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The advent of low cost, sophisticated, microprogrammable, LSI microprocessors has renewed interest in multiple-computer systems. This paper suggests a method of implementing microprogrammable microcomputer systems as a sophisticated tool (emulators) for decreasing the economic risk involved in development of large computer networks. Two levels of emulation are proposed for different network configurations. At the first level each microprocessor emulates one of the large computers in the rea ...

- 4 Techniques for Fast Transient Fault Grading Based on Autonomous Emulation 
Celia Lopez-Ongil, Mario Garcia-Valderas, Marta Portela-Garcia, Luis Entrena-Arrotones
March 2005 Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '05

Publisher: IEEE Computer Society

Full text available:  pdf(97.22 KB) Additional Information: [full citation](#), [abstract](#), [index terms](#)

Very deep submicron and nanometer technologies have increased notably integrated circuit (IC) sensitiveness to radiation. Soft errors are currently appearing into ICs working at earth surface. Hardened circuits are currently required in many applications where Fault Tolerance (FT) was not a requirement in the very near past. The use of platform FPGAs for the emulation of single-event upset effects (SEU) is gaining attention in order to speed up the FT evaluation. In this work, a new emulation sy ...

- 5 An insight into PDP-11 emulation 
 **J. C. Demco, T. A. Marsland**
September 1976 Proceedings of the 9th annual workshop on Microprogramming MICRO 9

Publisher: ACM Press

Full text available:  pdf(430.81 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In order to evaluate the Nanodata QM-1 as a universal host computer, an emulator for a contemporary computer, the PDP-11, was designed and constructed. It was required that the emulator be functionally equivalent to the target, without making excessive sacrifices in emulation speed. Some properties of emulation hardware necessary to achieve these goals are identified. In addition, the paper describes a monitor designed to support different emulators concurrently on a single host machine.

- 6 Fast development of source-level debugging system using hardware emulation (short paper) 
 **Sang-Joon Nam, Jun-Hee Lee, Byoung-Woon Kim, Yeon-Ho Im, Young-Su Kwon, Kyong-Gu Kang, Chong-Min Kyung**
January 2000 Proceedings of the 2000 conference on Asia South Pacific design automation ASP-DAC '00

Publisher: ACM Press

Full text available:  pdf(204.60 KB) Additional Information: [full citation](#), [references](#)

- 7 A user-microprogrammable, local host computer with low-level parallelism 
 **Shinji Tomita, Kiyoshi Shibayama, Toshiaki Kitamura, Toshiyuki Nakata, Hiroshi Hagiwara**
June 1983 ACM SIGARCH Computer Architecture News , Proceedings of the 10th annual international symposium on Computer architecture ISCA '83, Volume 11 Issue 3

Publisher: IEEE Computer Society Press, ACM Press

Full text available: [pdf\(708.91 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper describes the architecture of a dynamically microprogrammable computer with low-level parallelism, called QA-2, which is designed as a high-performance, local host computer for laboratory use. The architectural principle of the QA-2 is the marriage of high-speed, parallel processing capability offered by four powerful Arithmetic and Logic Units (ALUs) with architectural flexibility provided by large scale, dynamic user-microprogramming. By changing its writable control storage dy ...

Keywords: Firmware engineering, High-level language computer, Local host computer, Micropogrammable computer, Parallel processing

8 Solemn: Solaris Emulation Mode for Sparc Sulima

Bill Clarke

April 2004 **Proceedings of the 37th annual symposium on Simulation ANSS '04**

Publisher: IEEE Computer Society

Full text available: [pdf\(160.28 KB\)](#) Additional Information: [full citation](#), [abstract](#), [index terms](#)

In this paper we present Solemn, a new user-level simulationmode for Sparc Sulima, a SPARC V9 complete machinesimulator. Solemn extends Sparc Sulima allowing it tosimulate at user-level an unmodified Solaris executable: 32or 64-bit, and statically or dynamically linked. This yieldssome advantages over both complete machine simulatorsand traditional system call emulation. To do this, Solemnmanages the virtual address space and files that the simulatedprogram requires, and intercepts and emulates ...

9 On hardware enhanced 80386 software emulation, compiled emulation, a program

 distribution language, and pack computers

S. Lass

September 1989 **ACM SIGARCH Computer Architecture News**, Volume 17 Issue 5

Publisher: ACM Press

Full text available: [pdf\(218.87 KB\)](#) Additional Information: [full citation](#), [index terms](#)

10 Debug Support, Calibration and Emulation for Multiple Processor and Powertrain Control SoCs

A. Mayer, H. Siebert, K. D. McDonald-Maier

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 3 DATE '05**

Publisher: IEEE Computer Society

Full text available: [pdf\(222.95 KB\)](#) Additional Information: [full citation](#), [abstract](#), [index terms](#)

The introduction of complex SoCs with multiple processor cores presents new development challenges, such that development support is now a decisive factor when choosing a System-on-Chip (SoC). The presented developments support strategy addresses the challenges using both architecture and technology approaches. The Multi-Core Debug Support (MCDS) architecture provides flexible triggering using cross triggers and a multiple core break and suspend switch. Temporal trace ordering is guaranteed down ...

11 A Diagnostic Emulator for HEAO software development



Peter H. Beer, Kenneth J. Hupf

July 1976 **ACM SIGSIM Simulation Digest , Proceedings of the 4th symposium on Simulation of computer systems ANSS '76**, Volume 7 Issue 4

Publisher: IEEE Press, ACM Press

Full text available: [pdf\(701.56 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Diagnostic Emulation is the application of microprogramming to the emulation of an operational computer to support software development and verification for that computer. A conventional technique, Interpretive Computer Simulation (ICS), has been used for many years in support of such software development and verification efforts. The ICS method is becoming less cost effective. For the development of attitude control software for NASA's High Energy Astronomical Observatory (HEAO) diagnostic ...

12 Performance evaluation and improvement of a dynamically microprogrammable computer with low-level parallelism

 Shinji Tomita, Kiyoshi Shibayama, Toshiaki Kitamura, Hiroshi Hagiwara

November 1980 **ACM SIGMICRO Newsletter , Proceedings of the 13th annual workshop on Microprogramming MICRO 13**, Volume 11 Issue 3-4

Publisher: IEEE Press, ACM Press

Full text available: [pdf\(1.21 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

A new microprogrammable computer with low-level parallelism was built and has been utilized as a research vehicle for solving different classes of research-oriented applications such as real-time processings on static/dynamic images, pictures and signals, and emulations of both existing and virtual machines including high (intermediate) level language machines. The design goal of a research-oriented computer, QA-1, was to achieve a high degree of processing power and system flexi ...

13 Virtual square (V^2) in computer science education

 Renzo Davoli, Michael Goldweber

June 2005 **ACM SIGCSE Bulletin , Proceedings of the 10th annual SIGCSE conference on Innovation and technology in computer science education ITiCSE '05**, Volume 37 Issue 3

Publisher: ACM Press

Full text available: [pdf\(93.04 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

It is common to name as *virtual* the imaginary space that can be created by software using computers and networks. This space is not only a set of processing and communications means and methods but it is also a space where humans can "meet," exchange ideas, leave messages etc. Students in computer science must learn how to design, implement, manage and debug the systems and networks that create this virtual space. Furthermore, CS students need an experimental environment --a playground-- ...

Keywords: administration, laboratory, networking, operating systems, security, teaching, virtual machine

14 Advances in accelerated simulation: Communication-efficient hardware acceleration for fast functional simulation

 Young-II Kim, Wooseung Yang, Young-Su Kwon, Chong-Min Kyung

June 2004 **Proceedings of the 41st annual conference on Design automation DAC '04**

Publisher: ACM Press

Full text available: [pdf\(199.10 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents new technology that accelerates system verification. Traditional methods for verifying functional designs are based on logic simulation, which becomes more time-consuming as design complexity increases. To accelerate functional simulation, hardware acceleration is used to offload calculation-intensive tasks from the software simulator. Hardware accelerated simulation dramatically reduces the simulation time. However, the communication overhead between the software simulator a ...

Keywords: communication overhead, functional verification, simulation acceleration

15 Applying parallel discrete event simulation to network emulation

Rob Simmonds, Russell Bradford, Brian Unger

May 2000 **Proceedings of the fourteenth workshop on Parallel and distributed simulation PADS '00**

Publisher: IEEE Computer Society

Full text available:  [pdf\(767.64 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The simulation of wide area computer networks is one area where the benefits of parallel simulation have been clearly demonstrated. Here we present a description of a system that uses a parallel discrete event simulator to act as a high speed network emulator. With this, real Internet Protocol (IP) traffic generated by application programs running on user workstations can interact with modelled traffic in the emulator, thus providing a controlled test environment for distributed app ...

Keywords: Internet protocol (IP), computer network emulation, conservative protocol, critical channel traversing, parallel discrete event simulation (PDES), real-time simulation

16 Evaluation of alternate data base machine designs

 V. Vemuri, R. A. Liuzzi, J. P. Cavano, P. B. Berra

March 1980 **ACM SIGIR Forum , Proceedings of the fifth workshop on Computer architecture for non-numeric processing CAW '80**, Volume 15 Issue 2

Publisher: ACM Press

Full text available:  [pdf\(788.11 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The purpose of this paper is to point out the need for performance evaluation measures and techniques suitable for the evaluation of specialized architectural features in nonnumeric applications. Toward this end, problems associated with the use of data base machines are examined at three levels of detail: the user level, the system level and the device level.

17 Microarchitecture-level power analysis and optimization techniques: Hybrid simulation for embedded software energy estimation

 Anish Muttreja, Anand Raghunathan, Srivaths Ravi, Niraj K. Jha

June 2005 **Proceedings of the 42nd annual conference on Design automation DAC '05**

Publisher: ACM Press

Full text available:  [pdf\(1.01 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Software energy estimation is a critical step in the design of energy-efficient embedded systems. Instruction-level simulation techniques, despite several advances, remain too slow for iterative use in system-level exploration. In this paper, we propose a methodology called *hybrid simulation*, which combines instruction set simulation with selective native execution (execution of some parts of the program directly on the simulation host computer), thereby overcoming the disadvantages of in ...

Keywords: embedded software, energy estimation, energy macromodels, hybrid simulation, pointers analysis

18 EASY—an operating system for the QM-1

Charles W. Flink

 September 1977 **ACM SIGMICRO Newsletter , Proceedings of the 10th annual workshop on Microprogramming MICRO 10**, Volume 8 Issue 3

Publisher: IEEE Press, ACM Press

Full text available:  pdf(733.19 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The Emulation Aid SYstem is a virtual machine monitor for the Nanodata QM-1 microprogrammable computer. The system is designed to provide the user with an interactive interface for the development and subsequent use of emulations on the QM-1. EASY provides integrated support for: 1) interactive control of multiple, concurrently resident, virtual computers implemented via emulation, 2) input/output from emulations (virtual I/O) to the various real peripherals of the QM-1, and 3) diagnostic d ...

Keywords: Emulation, Intermediate language machines, Microprogramming, Nanodata QM-1, Software engineering, Virtual machine monitors, Virtual machines

19 Implementation aspects of a SPARC V9 complete machine simulator 

Bill Clarke, Adam Czezowski, Peter Strazzdins

January 2002 **Australian Computer Science Communications , Proceedings of the twenty-fifth Australasian conference on Computer science - Volume 4 ACSC '02**, Volume 24 Issue 1

Publisher: Australian Computer Society, Inc., IEEE Computer Society Press

Full text available:  pdf(1.33 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper we present work in progress in the development of a complete machine simulator for the UltraSPARC, an implementation of the SPARC V9 architecture. The complexity of the UltraSPARC ISA presents many challenges in developing a reliable and yet reasonably efficient implementation of such a simulator. Our implementation includes a heavily object-oriented design for the simulator modules and infrastructure, caching of repeated computations for performance, adding an OS (system call) emu ...

Keywords: SMP, SPARC V9 ISA, UltraSPARC, complete machine simulator, execution-driven simulation, object-oriented design

20 The Kiewit network: a large AppleTalk internetwork 

 R. E. Brown

August 1987 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM workshop on Frontiers in computer communications technology SIGCOMM '87**, Volume 17 Issue 5

Publisher: ACM Press

Full text available:  pdf(1.42 MB) Additional Information: [full citation](#), [abstract](#), [index terms](#)

Dartmouth College's Kiewit Network connects nearly all of the computing resources on the campus: mainframes, minicomputers, personal computers, terminals, printers, and file servers. It is a large internetwork, based on the AppleTalk protocols. There are currently over 2900 AppleTalk outlets in 44 zones on campus. Over 90 minicomputers act as bridges between 177 AppleTalk twisted pair busses. This paper describes the extent and facilities of the current network; the extensions made to the A ...

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 IPSJ : Information Processing Society of Japan
 SIGDA: ACM Special Interest Group on Design Automation
 IEICE : Inst of Electronics, Info & Communication Engineers

Publisher ACM Press New York, NY, USA

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Full text available:  [pdf\(414.73 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

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